A Holistic Approach Towards a Unified CpE Laboratory Platform

Peter Athanas and Cameron Patterson
Virginia Tech Department of Electrical and Computer Engineering
Blacksburg, Virginia
{athanas,cdp}@vt.edu

Introduction

At the beginning of the 2006-2007 academic year, the Virginia Tech Bradley Department of Electrical Engineering deployed an instructional plan that focused on unifying most of the Computer Engineering undergraduate laboratories. In this plan, the undergraduate computer engineering courses that had a laboratory component were restructured so that instead of being independently designed and operated, they would have a common foundation -- a common laboratory hardware platform satisfying the needs of all of the instructional exercises. This plan offers many advantages related course continuity, exercise quality, and most importantly, laboratory management and logistics. Even though the focus of this renovation plan was on the CpE program, all ~1000 undergraduates in the Virginia Tech ECE program are affected since the courses addressed in the plan are part of the common core shared among EE and CpE students. The plan shifts some of the burden of laboratory maintenance traditionally borne by the department onto the students by requiring each student to purchase a commodity high-performance FPGA-based single-board computer. Course instructors provide a flash image to the students that personalizes the board for the activities of a given course. While the plan is riddled with a number of logistical surprises, it offers several advantages that far outweigh the administrative costs. This paper provides a brief overview of the underlying motivations, logistics, and lessons learned involved in the deployment of this plan.

Background

The Virginia Tech ECE program is one of the larger undergraduate programs in the nation with roughly 1000 undergraduates and 75 faculty. The students are divided roughly equally between electrical engineering and computer engineering. Prior to the unification plan presented here, our undergraduate curriculum was not unlike most EE/CpE curricula, and retains a strong emphasis on embedded systems. The department's lab-oriented courses were originally created in isolation, and often within the time and resource constraints of the department instructional laboratories. For example, the senior-level digital design course utilized instructional lab stations instrumented with an FPGA board for performing experiments. The administrative overhead required to manage the resources for each of the course laboratory requirements remains costly – both in hardware resources and staff manpower.

Virginia Tech has always been fairly progressive in instructional computing. For example, Virginia Tech was one of the first universities to have a computer requirement for all incoming freshmen in the early 1990's, which later became a laptop requirement. The trend continues this year with all incoming freshmen required to have a tablet convertible computer -- a necessity for participating in freshman classroom exercises. While there are plenty of universities that require students to purchase hardware boards as part of a requirement for a class, the plan presented here is fairly unique in the fact that the same hardware board is used throughout the undergraduate curriculum, beginning with their first freshmen programming class, and extending through the senior-level capstone design classes. Since the designers of this plan wanted a single hardware platform to satisfy multiple courses, it was important that a highly flexible board be chosen. This naturally guided us in choosing an FPGA-based platform instead of a traditional microprocessor-based "trainer". It was also necessary to pick a platform that was capable of performing a wide diversity of experiments, suggesting a board with a variety of integrated peripherals and opportunity for expansion.

This is likely characterized less as of a revolutionary change in the ECE curriculum, but more of an evolutionary change. There are several factors that aligned at this point in time that ultimately made this a viable alternative for deployment. The first is university economics. Maintaining an instructional laboratory is expensive, and is often easy targets when department budget cuts are imposed. Nonetheless, campus laboratories are a necessary component for ECE education, yet a solution that promotes laboratory work outside of the campus environment seems to benefit everyone.

The second factor is student economics. It is unfair to impose a large financial burden onto the students, yet the cost of a highly capable FPGA board has been steadily declining. A decade ago, a platform with at least 100,000 gates would cost tens of thousands of US dollars. Today, a highly capable half-million gate board costs about as much as a textbook, which has been deemed an important metric, and the upper bound on the charges an instructor could impose on a student. Furthermore, the "cost-of-a-textbook" metric was also considered the threshold that would enable us to migrate to new platforms as they became available in the marketplace. While the students will likely be able to use the same board in multiple subsequent semesters, we make no promises of this when they make purchase. This allows us to role-in a new hardware platform in a single semester without stirring resentment among the student population.

Third, software tools and development environments have advanced nicely in the past decade. We've reached the point where an instructor can have students manipulate the logic within their board, but hide the underlying processes of FPGA design. In fact, the tools have evolved to the point where the platform can be completely abstracted. This is an essential factor that allows the faculty to engage freshmen with a motivating laboratory environment.

And finally, the fourth factor is economy-of-scale. The logistics of running a sizable ECE program can be overwhelming. Having a single platform that supports most if not all of an undergraduate program greatly simplifies the procurement, student support, testing, and hardware replacement process. It also helps faculty maintain their sanity by minimizing the needed multi-tasking between the multitude of course structures. Frankly, and generally speaking, students are more adept in embracing new development tools and environments than faculty. A one-size-fits-all approach works well with students, faculty, support staff, and outside hardware suppliers.

Deployment

In the fall of 2006, Virginia Tech required all incoming freshmen to purchase a supplemental hardware platform. Furthermore, sophomores, juniors, and seniors enrolled in five computer engineering courses were also required to purchase a supplemental hardware platform. The platform we chose was the Digilent Spartan3E Starter Kit [1,3]. While there are several competing platforms currently available, this one was chosen by the faculty with the expectation that it would best satisfy the broad requirements of all the undergraduate CpE courses. The specifications of this board can be found on the Digilent website [3], yet the properties that influenced the Virginia Tech decision process are summarized in Table 1.

Table 1: Factors that were used in choosing a hardware platform.

INFLUENTIAL HARDWARE PROPERTIES OF THE DIGILENT S3E STARTER KIT
1. The Xilinx XC3S300E Spartan3E FPGA [4] provides sufficient "elbow-room" to hold multiple 32-bit processor cores if needed, along with a long list of peripherals. It is also sufficiently fast to satisfy the computing requirements of the upper-level embedded computing exercises.
2. It contains a variety of standard interfaces, providing the opportunity to make meaningful experiments (interfaces including multiple SPI devices, a variety of memory interfaces, serial, VGA, PS/2, and so on).
3. A sufficient number of human I/O devices, allowing instant gratification for the lower-level and introductory experiments (switches, rotary knob, push buttons, LEDs, and an LCD display).
4. A high-bandwidth USB port for fast downloading of programs and operating systems, and responsive debugging.
5. A 10/100 Ethernet PHY enables inter- and intra-group projects.
6. The ability to retain multiple FPGA configurations in non-volatile (flash) memory.
7. Ample room for expansion with simple header I/O, and more robust high-speed I/O through an FX2 edge connector.
8. The cost to the student is equivalent to the price of a typical engineering textbook.

In the initial deployment, five lab-oriented undergraduate courses were targeted. More that 300 boards were deployed in the Fall 2006 semester, and an additional 280 boards were deployed in the Spring 2007 semester. In the freshman *Introduction to C/C++ Programming* course, the boards were statically configured with a 32-bit MicroBlaze processor [2] augmented with a variety of peripherals. Students used *gcc*, *g++*, along with a variety of debugging environment in their introductory exercises. The details of the underlying processor were unimportant at this level. The assignments were crafted to link to the large on-board DRAM bank (32 Mbytes), providing greater freedom in the choice of libraries and data sets. The junior-level *Microprocessors* class used an assortment of instructor-prepared processor configurations, allowing a variety of experiments in interfacing and comparative architectures. The senior-level *Digital Design II* course was the least impacted by the platform change since the course focuses on HDL design and synthesis on FPGAs. The senior-level *Embedded Systems* course is highly project oriented. Students fine-tune the instructor-provided processor configuration by adding custom peripherals, ultimately to interact in larger team-oriented projects. Also, the students in this course are exposed to a variety of RTOS environments layered on the MicroBlaze processor. The senior-level technical elective, *Hardware-Software Co-Design* used specialized compilers and synthesis environments, ultimately targeting the Digilent board. These courses are summarized in Table 2. Courses that will likely be integrated into this program are listed in italics in the table.

Conclusion

Virginia Tech is currently in the second semester of this program. Overall, the feedback has been positive. The students at all levels have been complacent since the boards chosen are robust and exhibit virtually no failures. Software is distributed via DVD, eliminating the need of lengthy downloads. Many students from the Fall semester had the opportunity to sell their boards to new students requiring a board in the subsequent Spring semester, but chose to keep their board for continued exploration and home projects. In this period, nine faculty members have come up-to-speed on the hardware and software, reporting few problems. Furthermore, the quality of the experiments offered to the students is much higher than those prior to this program. Virginia Tech will continue with this program in the years to come.

References

[1] Spartan-3E Starter Kit Board User Guide UG230 (v1.0) March 9, 2006,
http://www.xilinx.com/bvdocs/userguides/ug230.pdf

[2] MicroBlaze Processor Reference Guide Embedded Development Kit EDK 8.2i
UG081 (v6.0) June 1, 2006.,
http://www.xilinx.com/ise/embedded/mb_ref_guide.pdf

[3] The Digilent Spartan3E Starter Board,
http://digilentinc.com/Products/Detail.cfm?Prod=S3EBOARD&Nav1=Products&Nav2=Programmable

[4] Xilinx DS312 Spartan-3E FPGA Family Data Sheet,
http://direct.xilinx.com/bvdocs/publications/ds312.pdf