

VTsim: A Virtex-II Device Simulator

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Abstract

This paper introduces VTsim, a device simulator for Xilinx Virtex-II FPGAs. VTsim is currently a globally synchronous event-driven device simulator modeled at the CLB level. Through use of JBits3 and ADB, VTsim provides designers with the ability to simulate all resources within an FPGA via a virtual device. The simulator has been designed for rapid response, low memory usage, and ease of interaction. VTsim is part of the JHDLBits open-source project geared at providing enhanced control of resource manipulation, placement, and routing.

1. Introduction

FPGA tool suites try to manage the complexity of large designs. Many implementation flows include behavioral simulators that allow the user to verify the functionality of a design, typically using an architecture-independent model. However, these flows assume that a verified design will work in the hardware as intended. If the design does not function correctly in hardware, then several possible problems arise: The FPGA may be faulty; the implementation tools may have inferred, placed, and routed the logic differently than intended; or a flaw in the design was missed during testing. VTsim was designed to resolve these problems by providing a window into the FPGA fabric via a virtual device. By using VTsim, a designer can access all resource values within the virtual FPGA at any given time, view the state of flip-flops and lookup tables, or examine values on a routed wire. The only required input to VTsim is a valid bitstream, which can be generated from any tool suite.

VTsim is useful in reconfigurable designs where logic blocks are inserted and removed based on specific system states. In designs that use partial reconfiguration,

the placement of certain logic blocks is fixed, which allows the designer to reconfigure a small portion of the chip without affecting the overall design. Unfortunately, the majority of simulators currently available do not have adequate support for reconfigurable designs. Because VTsim works at the bitstream level, partial reconfiguration may be simulated.

The main goal of VTsim was to create a Java-based virtual FPGA to model all resources within any Virtex-II FPGA, initially without timing support. A secondary goal was to design the simulator framework such that a large portion of the simulator could be ported for use with future FPGA architectures other than the Virtex-II family. VTsim is integrated into the open-source (sourceforge.net) JHDLBits [7] design suite, allowing simulation in either the JHDL [4] to JBits [2] flow, or as a standalone tool.

2. JBits and ADB Background

JBits is a Java-based API that provides access to every configurable resource in a Xilinx FPGA. Device resources may be programmed and probed at run-time, even with the FPGA active in a working system. The JBits3 SDK [9] provides support for Virtex-II FPGAs, unlike the Virtex-based JBits2.8 release.

Although JBits3 is a complete API for examining and modifying device configuration, it does not include a device simulator or router as in the previous JBits2.8 release. JBits2.8 included VirtexDS, a high performance device simulator for the Virtex family of FPGAs [6], and JRoute, a run-time reconfigurable router [5]. The absence of a device simulator in JBits3 hinders design verification and the development of run-time reconfigurable systems.

Although no direct comparison can be made between VirtexDS and VTsim because the two operate on different architectures (VirtexDS supports Virtex FPGAs and VTsim supports Virtex-II FPGAs), there

are some similarities between the device simulators. Both simulators are event-based, with two logic states [1]; require only an input bitstream for simulation, and support all devices within the designated family. Unlike VirtexDS, VTsim currently does not have support for the Xilinx HardWare Interface (XHWIF) [3], does not allow simulation of asynchronous circuits, and does not support timing information although timing support is expected in future versions of VTsim. Two features not available in VirtexDS will be present in VTsim: support for input stimuli files and the ability to analyze circuits containing multiple clocks.

Although JBits3 does not include a router, it does include a router interface allowing users to plug-in their own router. An example is the Alternate Wire Database (ADB) [8] supporting Virtex, Virtex-E, Virtex-II, and Virtex-II Pro FPGAs. Unlike JRoute in JBits2.8, ADB provides complete device coverage and is very memory-efficient. ADB does not perform timing-driven routing; however, this simplification enables ADB to route nets quickly.

3. Implementation

The simulation process begins by invoking the ADB tracer on the bitstream to be simulated. After the tracer builds its database, the simulator constructs a netlist of the internal connections between all tiles. An optional JHDLBits simulation file can be used to provide specific information such as net names and placement information. Next, the tiles appearing in the netlist are configured within the virtual device using JBits. After the device has been completely configured, all non-clocked elements are evaluated to ensure device stability and that the proper value is on each simulation net.

Simulation begins by triggering an event on the system clock. This event causes all clocked elements connected to the clock to be updated. A new event is generated if the simulation net connected to the output of a clocked element changes. Once a change on a net occurs, all CLBs connected to the net are placed on the event queue provided they are not already present on the queue. The simulator removes and evaluates the first CLB on the queue and places any new events back onto the queue. When the queue is empty, the simulator can either write the updated results back to a bitstream, or allow GUI access to the modified information.

4. Results and Conclusions

VTsim has been used successfully to verify simple designs such as adders, counters and shift chains. The simulator is currently being used in the JHDLBits project to provide quick design feedback. The next objective in the simulator development is to decrease memory usage, improve execution time, and provide a more flexible interface. Future work on VTsim should provide support for XHWIF, asynchronous circuits, and timing information.

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